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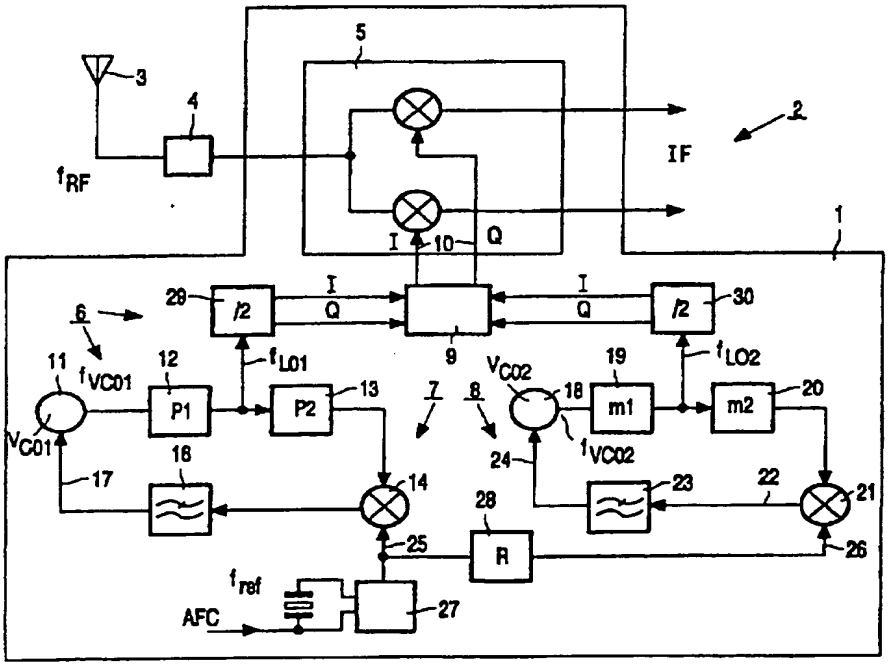
(54) Title: A COMMUNICATION SYSTEM, A COMMUNICATION DEVICE AND A FREQUENCY SYNTHESIZER

(57) Abstract

A frequency synthesizer is presented comprising RF mixer means, and local oscillator means coupled to the RF mixer means. The local oscillator means comprises local oscillator mixer means coupled to the RF mixer means as well as band and channel selection means coupled to the local oscillator mixer means. This concept allows the frequency synthesizer to be integrated in a way wherein power consumption can be made very low while complying with required signal to noise and spurious to noise ratios. Advantages are related to applications in integrated low power communication devices.



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"A communication system, a communication device and a frequency synthesizer"

The present invention relates to a frequency synthesizer outlined in the preamble of claim 1.

The present invention further relates to a communication system and a communication device.

J. Crols et al., describes in "A Single-Chip 900 MHz CMOS Receiver Front-End with High Performance Low-IF Topology", IEEE Journal of Solid State Circuits, vol. 30, No. 12, December 1995, pp 1483-1492, the realization of a fully integrated high performance receiver comprising an RF (Radio Frequency) frequency synthesizer for frequency down conversion. Apart from the required degree of integration of the several functional circuits in a communication device or system comprising such a frequency synthesizer one of the major problems not addressed by Crols et al. is the relatively high power consumption of the frequency synthesizer(s).

It is an object of the present invention to provide a frequency synthesizer having a reduced power consumption, without affecting the required degree of integration.

To this end the frequency synthesizer according to the invention has the characterising features outlined in claim 1.

It is noted here that it is known from JP-A-63-84320 to include in a frequency synthesizer a frequency multiplier connected single local oscillator mixer means which is coupled to a reference crystal oscillator phase locked loop controlled parallel arrangement of a frequency variable phase locked loop and a third phase locked loop. This known microwave band frequency synthesizer does not disclose RF mixer means and only discloses one frequency variable phase locked loop, whereas the other parallel phase locked loop is supposed to provide a fixed frequency and does therefore not provide a simultaneous band selection.

It is an advantage of the frequency synthesizer according to the invention

that due to the relatively high reference frequency the band and simultaneously active channel selection at this reference frequency provides possibilities in the practical realisation of the frequency synthesizer to decrease power consumption, which is inverse proportional to its working frequency. In addition this synthesizer concept has inherent possibilities to relax VCO noise requirements, that is the presence of side band noise in the spectrum of oscillators, such as voltage controlled oscillators (VCOs), applicable in the local band and channel means. The reduced noise requirements reduce the said decreased power consumption further, because the higher the signal to noise ratio is the higher the power consumption has to be to comply with such ratio.

As a consequence in portable or mobile applications of the frequency synthesizer such as in pagers, portable telephones etcetera the life-time of batteries included in communication devices has been increased.

It is a further advantage of the frequency synthesizer according to the invention that if an I and Q pair of paths is being used in the local oscillator means, applicable accurate wide-band 90 degrees phase shifters can easily be integrated as divide by two means which can be integral part of phase locked loop dividers usable in the local oscillator mixer means. This obviates the need for accurate external phase shifters in the local oscillator mixer means which would require tuning of components, especially in case of multi-band applications.

In an embodiment of the frequency synthesizer according to the invention phase locked loops, in particular separate phase locked loops are being used. This gives rise to a new architecture when it comes to the synthesized radio concept in that a first phase locked loop provides a first local oscillator signal at a high frequency, which first phase locked loop may be wide-band in order to clean the above mentioned VCO side band noise, which may now originate from a relatively noisy, and thus low power, fully integrated first phase locked loop. Simultaneously a second local oscillator signal which is mixed in the local oscillator means with the first local oscillator signal provides channel selection.

According to a still further embodiment of the frequency synthesizer according to the invention a frequency dividing means is being used coupled between the local oscillator mixer means and the two separate phase locked loops. As a advantageous consequence the respective frequency division ratios (which ratios in particular are 2) of the frequency dividing means reduce the side band noise of each of the VCOs. Especially for fully integrated LC oscillators the high oscillating frequency results in relatively low power consumption of the VCO due to the increased Q-factor of the applied coils. The relatively

high VCO frequency asks for smaller self inductances which allows for integration on less chip area.

In a preferred embodiment the frequency dividing means generally embodied as easy to integrate dividers have programmed frequency division ratios. This offers great flexibility in the practical application and in the frequency band and selection values of the frequency synthesizer according to the invention upon application in (tele)communication devices and systems, such as radio transmission systems, audio- and/or video systems, control systems, telemetry systems, local area networks, wide area networks, cordless or cellular pager or telephone systems, car-transceivers for mobile communication, or a transceivers in radio base stations of a mobile networks.

At present the frequency synthesizer according to the invention and its applications in a variety of types of communication devices and systems will be elucidated further together with its additional advantages while reference is being made to the appended drawing, wherein similar components are being referred to by means of the same reference numerals.

In the drawing:

Fig. 1 shows a detailed arrangement of a possible embodiment of the frequency synthesizer according to the invention here applied in a receiver;

Fig. 2 shows a possible double quadrature arrangement of mixers in a local oscillator mixer means for application in the frequency synthesizer of fig. 1; and

Fig. 3 schematically shows a (tele)communication system having communication devices provided with a frequency synthesizer according to the invention.

Fig. 1 shows a frequency synthesizer 1 applied in a receiver 2, which is partly shown. The receiver 2 comprises an antennae 3 coupled to filter and gain means 4, RF mixer means 5 coupled to the said means 4, and local oscillator means 6 coupled to the RF mixer means 5. The remaining parts of the receiver 2, which may be implemented either in an analog or digital way are known per se and therefore not described here. An RF signal (f_{RF}) received on the antennae 3 is filtered, amplified and mixed with a local oscillator signal from oscillator means 6 to yield a possible IF signal, and then processed further in the remaining part of the receiver 2. The receiver 2 can either be a embodied as a low-IF, zero-

IF, or as a IF receiver, such as a well known superheterodyne receiver. The RF mixer means 5 structure can include one mixer or a two parallel quadrature mixer structure as shown in figure 1, whereas a four parallel quadrature mixer structure although possible seems less likely. Of course application of the frequency synthesizer 1 is possible with frequency down conversion as well as in frequency up conversion such as in transmitters, or in transceivers.

The local oscillator means 6 comprises band selection means in the form of a first local oscillator means 7 and channel selection means in the form of a second local oscillator means 8. The local oscillator means 6 further comprises local oscillator mixer means 9 coupled to the band and channel selection means 7 and 8. Depending on the embodiment of the RF mixer means 5 the local oscillator mixer means 9 thus provide a single or quadrature (I and Q) local oscillator signal at output 10 thereof, which output 10 is connected to the RF mixer means 5. The output 10 thus provides a local oscillator signal which simultaneously represents a band frequency as well as a channel frequency selection oscillator signal the operation whereof will be elucidated later on in this description.

The band and channel selection means are embodied as phase locked loops 7 and 8. The first phase locked loop (PLL) 7 comprises a first voltage controlled oscillator (VCO) 11 for providing a signal having a frequency f_{VCO1}, a first frequency divider 12 having a frequency division ratio P1 and connected to VCO 11 for providing a signal having frequency f_{LO1}. The signal f_{LO1} is fed through a second frequency divider 13 in the PLL 7 to a phase detector which may as shown in figure 1 be embodied as a simple first mixer 14 having an output 15 for providing a control signal through a loop filter 16 to a frequency control input 17 of the VCO 11. Divider 13 has a frequency division ratio P2. Similarly the second phase locked loop (PLL) 8 comprises a second voltage controlled oscillator (VCO) 18 for providing a signal having a frequency f_{VCO2}, a third frequency divider 19 having a frequency division ratio M1 and connected to VCO 18 for providing a signal having frequency f_{LO2}. The signal f_{LO2} is fed through a fourth frequency divider 20 in the PLL 8 to a further phase detector which may as shown in figure 1 be embodied as a simple second mixer 21 having an output 22 for providing a control signal through a loop filter 23 to a frequency control input 24 of the VCO 18. Divider 20 has frequency division ratio M2. Phase detectors, in this case mixers 14 and 21 have further inputs 25 and 26 respectively. In an embodiment the frequency synthesizer 1 comprises a stable reference oscillator, such as a crystal oscillator 27 providing a stable frequency f_{ref}, generally with an AFC for providing frequency offset compensation, which oscillator 27 is connected to input 25 and coupled to

input 26 through a fifth frequency divider 28 having a wanted frequency division ratio R.

Preferably any or each of the aforementioned dividers 12, 13, 19, 20, and 28 have programmable frequency division ratios (these may be integers or fractional numbers) which offers frequency choice flexibility. In particular the frequency division ratio of third frequency divider 19 is programmable such that for all frequency bands of the receiver or transmitter wherein the frequency synthesizer 1 is being applied an optimum frequency range for f_{VCO2} covering said bands can be chosen while the oscillating frequency range of VCO 18 remains the same.

The embodiment of the frequency synthesizer 1 as shown in figure 1 is also provided with further frequency dividing means 29 and 30 connected between the separate PLLs 7 and 8 respectively. These dividing means 29 and 30 easily provide - embodied as simply to integrate phase shifters- quadrature output signals usable as oscillator input signals for the possibly quadrature local oscillator mixer means 9, without the requirement to apply well known accurate 90 degrees phase shifters for providing the necessary quadrature oscillator signals to the local oscillator mixer means 9. Essentially the means 29 and 30 are to be considered as an easy implementation of preferably wide band phase shifters. Such phase shifters could comprise passive or active RC/LC networks for providing the mentioned quadrature output signals.

Figure 2 discloses a possible double quadrature arrangement of four mixers a, b, c, and d, whose inputs are connected to respective I and Q signals originating from said means 29 and 30 respectively, and whose outputs are connected to respective adder e and f, each having a respective output for providing the I and Q signals to output 10 of the local oscillator mixer means 10. In case the RF mixer means 5 shows a one mixer structure one of the adders e and f can be dispensed with and the pair of mixers connected thereto can be deleted. Depending on the signs of the addition in the adders e, f of the output signal(s) the output signal on output 10 provides rejection of either the upper or the lower frequency side band components $(f_{LO1})/2) +/- (f_{LO1}/2)$.

Table I hereunder specifies possible choices of operating frequencies for the embodiment as shown, which is particularly advantageous for paging operations in the RF frequency range from 130 MHz to 930 MHz, for instance.

f_{RF} [MHz]	f_{ref} [MHz]	f_{VCO1} [MHz]	P1	P2	f_{LO1} [MHz]	f_{LO2} [MHz]	M1	f_{VCO2} [MHz]
930	67	1600	1	24	1600	260	1	260
490			2	12	800	180	2	360
450						100	3	300
450			3	8	533	386	1	386
410						286	1	286
330			3	8	533	140	2	280
280			4	6	400	160	2	320
180			6	4	267	40	8	320
160						54	6	324
160			4	6	400	80	4	320
130						140	2	280

TABLE I

By changing the frequency division ratios P1 and P2, while keeping P1*P2 constant different LO1 frequencies can be generated for different frequency bands to be selected and covered. PLL 7 is wide band which is being determined by the loop filter 16 and the side band noise of VCO 11 is being cleaned up by the loop itself. A relatively high f_{ref} of 67 MHz is used to relax the spurious rejection requirements of the loop filter 16. Due to this high reference frequency the second PLL 8 is used for channel selection. The lower frequency choice of VCO 18 allows for the realisation of a low noise VCO 18 at relatively low power or the use of a relatively noisy, high frequency, VCO 18 in combination with the dividers 19 and 20. The divider 19 reduces the VCO's 18 side band noise by its frequency division ratio, which allows for a reduction in the power dissipation in the frequency synthesizer 1, because generally speaking the power dissipation of a VCO increases with its increasing carrier to noise ratio. Thus a low power easy to integrate solution is thus provided. At wish the output oscillator frequency f_{VCO2} of VCO 18 can advantageously be chosen around 2 GHz by increasing M1 with a factor 6 to 10.

Figure 3 shows a telecommunication system 31 comprising several transceivers 32 provided with one or more frequency synthesizers 1. The telecommunication system 31 can be a radio transmission system, audio- and/or video system, control system, telemetry system, a terrestrial/satellite system or a local area network. The transceivers 1 are

also applicable in cordless or cellular telephone systems, as well as in a handset, a car-transceiver for mobile communication, portable devices or a transceiver in a radio base station of a mobile network.

In view of the foregoing it will be evident to a person skilled in the art that various modifications may be made within the spirit and the scope of the present invention as hereinafter defined by the appended claims and that the present invention is thus not limited to the examples provided.

CLAIMS:

1. A frequency synthesizer comprising RF mixer means, and local oscillator means coupled to the RF mixer means, characterised in that the local oscillator means comprises local oscillator mixer means coupled to the RF mixer means as well as band and channel selection means coupled to the local oscillator mixer means.

2. A frequency synthesizer as claimed in claim 1, wherein the band and channel selection means comprises phase locked loop means.

3. A frequency synthesizer as claimed in claim 2, wherein the phase locked loop means comprises two separate phase locked loops.

4. A frequency synthesizer as claimed in claims 1, 2 or 3, wherein the frequency synthesizer comprises a stable reference oscillator coupled to the band and channel selection means.

5. A frequency synthesizer as claimed in claim 4, wherein the frequency synthesizer comprises frequency dividing means coupled between the local oscillator mixer means and the two separate phase locked loops.

6. A frequency synthesizer as claimed in the claims 2, 3, 4 or 5, wherein the phase locked loop means comprises further frequency dividing means.

7. A frequency synthesizer as claimed in claims 5 or 6, wherein the, possibly further, frequency dividing means are provided with dividers whose frequency division ratio is programmable.

8. A frequency synthesizer as claimed in claim 1, wherein that the RF mixer means and/or the local oscillator mixer means comprises single, quadrature or double quadrature mixer means.

9. A communication device comprising one or more of a transmitter, a receiver or a transceiver, each communication device comprising a frequency synthesizer as claimed in any one of the claims 1 to 8, the frequency synthesizer comprising RF mixer means, and local oscillator means coupled to the RF mixer means, characterised in that the local oscillator means comprises local oscillator mixer means coupled to the RF mixer means as well as band and channel selection means coupled to the local oscillator mixer means.

10. A communication device as claimed in claim 9, wherein the RF mixer means are embodied as zero-IF, low-IF, double conversion zero-IF, double conversion low-IF, or standard superheterodyne mixer means.

11. A communication system comprising at least one communication devices as claimed in claims 9 or 10, wherein communication system is a radio transmission system, an audio- and/or video system, a control system, a telemetry system, a terrestrial/satellite system, a local area network, a cordless or cellular pager or telephone system, a car-transceiver for mobile communication, or a transceiver in a radio base station of a mobile network.

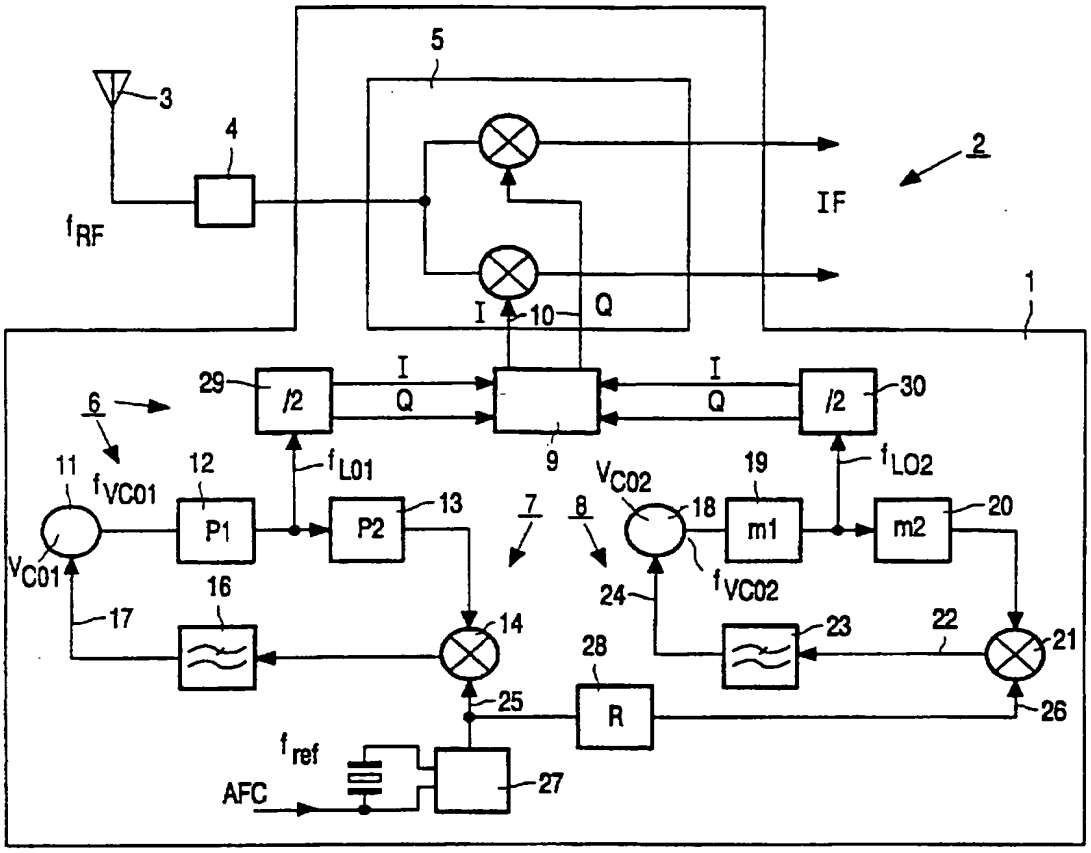
5
3
4
2
IF
f_{RF}
I
10
Q
1
6
29
/2
I
Q
I
Q
/2
30
11
f_{VC01}
12
f_{LO1}
9
V_{C02}
19
f_{LO2}
V_{C01}
P1
P2
13
7
8
18
m1
m2
20
16
f_{VC02}
24
17
14
23
22
21
28
25
R
26
f_{ref}
AFC
27

FIG. 1

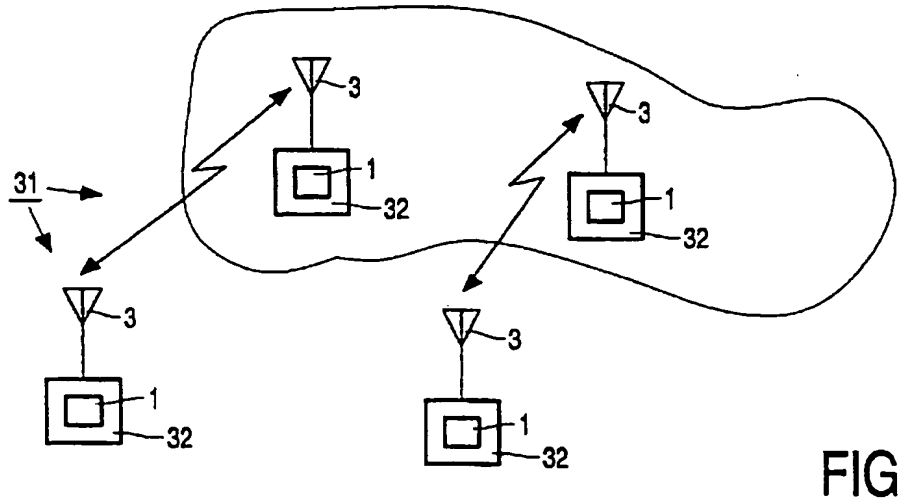
31
3
1
32

FIG. 3

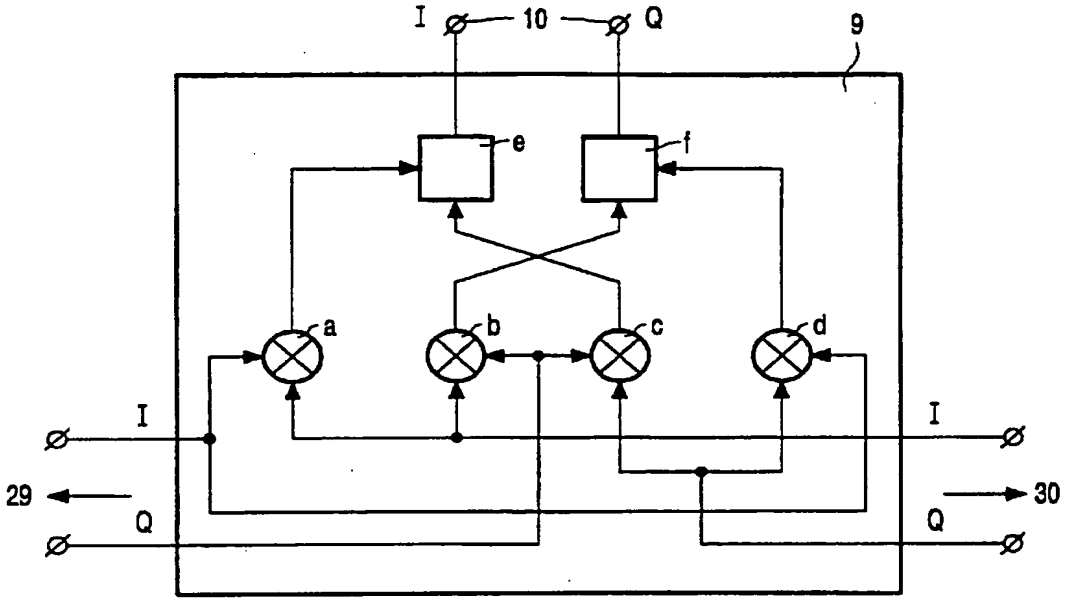

FIG. 2

INTERNATIONAL SEARCH REPORT

International application No.
PCT/IB 98/01907

A. CLASSIFICATION OF SUBJECT MATTER

IPC6: H03L 7/23 // H04B 1/00
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC6: H03L, H04B, H04N, H04Q

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

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Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

EDOC, WPIL, JAPIO, INSPEC

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4395777 A (RYUJI OKI ET AL), 26 July 1983 (26.07.83), figure 1, abstract --	1
A	US 5448763 A (STEVEN F. GILLIG), 5 Sept 1995 (05.09.95), see the whole document --	1
A	US 4245350 A (FREDERIC J. MOORE), 13 January 1981 (13.01.81), figure 1, abstract --	1

☐ Further documents are listed in the continuation of Box C. ☒ See patent family annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
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INTERNATIONAL SEARCH REPORT

Information on patent family members

07/04/99

International application No.
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